MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/23

ECE4116 DIGITAL COMPUTER DESIGN

(All Section / Groups)

07 JULY 2023
9:00 a.m. – 11:00 a.m.
(2 hours)

INSTRUCTIONS TO STUDENT

1. This Question paper consists of 4 pages, including the cover page and with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks, and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) A Boolean function F is given as

$F(x, y, z) = \sum m(0, 4, 5, 7)$

i. Construct the truth table for function F. [3 marks]

ii. Draw the logic circuit to implement function F with a 4-to-1 multiplexer and necessary logic gates. [4 marks]

iii. Write the VHDL entity and dataflow architecture for the logic circuit in Q1(a)(ii). [5 marks]

(b) Figure Q1(b) shows the Finite State Machine (FSM) chart of a sequential circuit with 2 inputs, W1 and W2, an output, Z.

(i) Draw the Algorithmic State Machine (ASM) chart for the circuit based on the FSM.

[5 marks]

(ii) Design the circuit using the One Flip-Flop Per State technique. Draw the circuit diagram.

[8 marks]

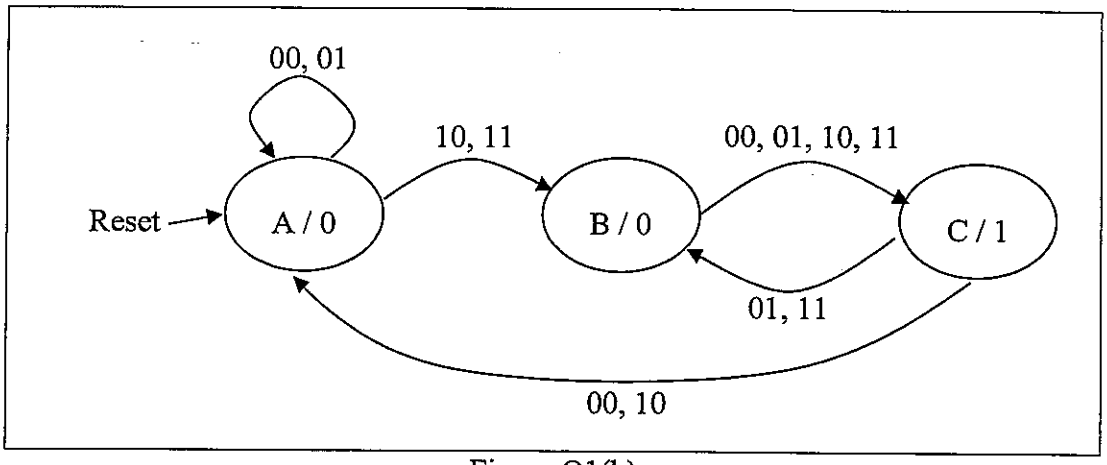

Figure Q1(b)

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Question 2

(a) A digital system has TWO (2) registers, *RA* and *RB*, and control signals *C*1, *C*2, and *C*3. The control signals is used to control the following register transfers:

$$C1: RA \leftarrow RB$$
$$C2: RA \leftarrow \overline{RB}$$
$$C3: RA \leftarrow RA + RB \quad ; \text{(logical } OR\text{)}$$

All the control signals are mutually-exclusive. If none of the control signals are '1', then no transfers occur. Design the logic circuit to implement the register transfers and draw the one-bit slice logic diagram.

[10 marks]

(b) List types of microoperations.

[3 marks]

(c) Given a 16K×8 RAM that is constructed by multiple 4K×8 RAM chips.

(i) Determine the number of address lines available on each 4K×8 RAM chip.

[2 marks]

(ii) Compute the number of address lines needed for the 64K×8 RAM

[2 marks]

(iii) Draw the 16Kx8 RAM block diagram using 4K×8 RAM chips with a decoder. Label all the address lines, data lines, and control inputs.

[8 marks]

Question 3

(a) Design and give the function of a 4-bit arithmetic circuit with two selection variables, S_1 and S_0, and two data inputs, A and B, that generates the following arithmetic operations:

S_1S_0	$C_{in} = 0$	$C_{in} = 1$
00	$F = A + B$	$F = A+B+1$
01	$F = A$	$F = A + 1$
10	$F = B$	$F = B + 1$
11	$F = A + B$	$F = A+B+1$

Draw the logic diagram for the design above assuming the data inputs are a typical single-bit stage. [11 marks]

(b) An instruction consisting of two words is kept in memory at the location denoted by the symbol W, which is a word. The symbol Y indicates the address field of the instruction, and it is stored in the W+1 position. The effective address, denoted by the letter Z, is where the operand used while the instruction was carried out is kept. A value denoted by X is stored in an index register. Indicate the method by which Z is derived from the other addresses if the addressing mode of the instruction is:

(i) Direct. [2 marks]

(ii) Indirect. [2 marks]

(ii) Relative. [2 marks]

(iii) Indexed. [2 marks]

Continued...

(c) Each instruction on a computer is exactly one word long and does not include a mode field. The word length of a computer is 32 bits, and there is no mode field. The register file inside the computer has a total of sixty-four different registers.

(i) For instruction with three register addresses and an 8-bit constant field, determine the maximum number of possible opcodes. [3 marks]

(ii) For an instruction format with two register addresses, one constant field and a maximum of 64 opcodes, what is the number of bits available for the constant field? [3 marks]

Question 4

(a) The sequence of four LDI instructions given in Table Q4(a) is fetched and executed by a RISC CPU with four pipeline stages.

Table Q4(a)

LDI	R1,2
LDI	R3,4
LDI	R5,6
LDI	R7,8

Manually simulate the execution by giving, for each clock cycle, the value in pipeline registers *PC*, *IR*, *Data A*, *Data B*, *Data F*, and the relevant register for each clock cycle. Assume that the first given instruction is at memory address *N*. All registers initially contain -1. [10 marks]

(b) For a RISC CPU with 4 pipeline stages, draw the execution diagram for the RISC program listed in Figure Q4(b) (with the contents of R5 nonzero after the subtraction), and indicate any data or control hazards that may present. [7 marks]

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SUB R5, R5, R1
BNZ R5, 000F
AND R6, R5, R2
OR  R2, R6, R1
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Figure Q4(b)

(c) Rewrite the RISC program in Figure Q4(b) using NOPs to avoid all data and control hazards, and draw the new execution diagram. [8 marks]

End of Paper